Design of Alloyed Junction Germanium Transistors for High-Speed Switching

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Alloyed-junction transistors hove been critically evaluated with respect to their potential use as high-speed switching devices. Limitations ore found to result from avolonche multiplication ond space charge layer widening which necessitate design compromises between high frequency and high voltoge circuit requirements. It is shown in this article thot n-p-n germonium tronsistors have an advantoge over p-n-p type beyond that expected from mobility considerations. The additionol advantage derives from differences in avolanche multiplication.

1.0 INTRODUCTION

The present trend in switching systems and computers is toward systems that operate at megacycle rates with pulse rise times in the vicinity of a tenth of a microsecond. In the attendant design of pulse-amplifiers, pulse-generators, and flip-flops there has arisen the need for high-speed junction transistors, particularly in cases where the device must switch high currents for extended periods of time. Roughly, devices are needed with alphas greater than 0.95 and frequency cut-offs of alpha in the range of 10 to 50 mc per second. In considering transistor structures for high pulse rate systems there are several contenders for further development, for example, grown-junction triodes and tetrodes, alloyed-junction triodes, and intrinsic-barrier transistors.[1] A comparison has to be made of the design possibilities and the relative merits of these devices when used as switches. The objective of this paper is to determine the applicability and limitations of alloyed-junction transistors in high-speed switching applications. Many of the considerations in the design of alloyed-junction transistors for switching are also important in large-signal transmission applications.

Alloyed junctions transistors have been extensively used in switching systems having a pulse rate below a megacycle per second with excellent

results which can be attributed to their low impedance in the ON condition when used as a switch, to their high OFF impedance and to the relatively small storage of minority carriers compared to grown junction transistors. In extending the operating range toward higher speeds, limitations are found to result from:

1. punch-through, the spreading of the collector junction space-charge-layer over to the emitter junction,[2]
2. avalanche multiplication of alpha which results in alphas greater than unity at collector voltages well below the theoretical breakdown voltage,[3, 4, 5, 6]
3. collector capacitance which in combination with the load resistance may severely limit pulse rise time, and
4. the practical limitation of reproducibly fabricating transistors with extremely narrow base layers. With increased understanding of the properties of junctions and transistors, it has become possible to determine whether a given set of circuit requirements can be met, even theoretically, by a proposed design. For example, the requirements may be that the device operate up to a certain voltage, that at this voltage the alpha remain below unity and the collector space charge region not punch through to the emitter, and that the frequency response be high enough for the application.

The maximum permissible base layer width is essentially fixed by the specified frequency cutoff. With this base width, the requirement that there be no punch-through at the highest operating voltage puts an upper limit on base resistivity, since the encroachment into the base layer of the collector space charge region is greater the higher the base resistivity. On the other hand, the requirement that the low-voltage alpha times the avalanche multiplication of the collector junction be less than unity, sets a lower limit on permissible collector body breakdown voltage. This limit, in turn, sets a lower limit on permissible base resistivity, since for an alloyed structure the collector breakdown voltage is nearly a linear function of base resistivity. It is only for base resistivities between these two limits, if such a region exists, that designs are possible.

Since in germanium holes produce greater avalanche multiplication than electrons in a given electric field,[5] there exists under the above condition a greater difference in the maximum obtainable frequency cutoff of alpha between npn and pnp transistors than would be expected merely on a basis of the difference in mobility between holes and electrons.

The most general transistor design considerations for a switch involve

the OFF impedance, the ON impedance, the switching time, the current carrying ability, and the maximum open circuit voltage. As implied above, important interrelations between these switch parameters exist which limit the range of possible design. Furthermore, in order to carry through a transistor switch design it is necessary to know how the switch parameters are related to the terminal behavior of the transistor. The large-signal behavior of junction transistors has been discussed in two previous papers, and it has been found possible to relate the large-signal behavior to easily measurable transistor parameters which are in turn intimately related to the physics and structure of the transistor.[7]

The plan of this paper will be: (1) to review the switch requirements and to specify them in terms of transistor device parameters, (2) to show how the device parameters are related to the structure, and (3) to indicate the method of obtaining a design to meet a given set of switch requirements or to determine whether or not such a design is possible. The discussion will be primarily in terms of a common-emitter pulse amplifier since this circuit has proven to be the one which is most widely used and since it exemplifies the problems encountered in transistor design for switching applications.

2.0 SWITCH REQUIREMENTS

2.1 *OFF Impedance*

In the common-emitter pulse amplifier circuit (see Fig. 1) means are usually supplied to reverse bias both the collector and emitter junctions in the absence of a driving pulse. Under these conditions the collector current is given by[7]

$$I_C = \frac{I_{CO}(1 - \alpha_I)}{1 - \alpha_N \alpha_I} \tag{1}$$

where α_N and α_I are the normal and inverted alphas, respectively. In order to make this current as small as possible it may be desirable to have an alloyed-junction transistor with an emitter junction which is larger in diameter than the collector, thus having α_I greater than α_N. In most cases this is not feasible because α_N must be large for other reasons. About the best that can be done is to use a symmetrical structure with $\alpha_N = \alpha_I$. The collector current in the OFF condition is then given by

$$I_C = \frac{I_{CO}}{1 + \alpha_N} \tag{2}$$

which for high alpha transistors approaches $\frac{1}{2}I_{co}$, corresponding to an OFF impedance of $2Vc/I_{co}$. The value of I_{co} increases to some extent with collector voltage due to avalanche multiplication. In many cases there is also a surface leakage current which is not subject to analysis.

In some applications the ac impedance of the switch in the OFF condition is of great importance. It has been found possible to fabricate junction devices in which the slope of the reverse junction characteristic is consistantly greater than 25 megohms. In this event the junction capacitance places an upper limit on the OFF impedance.

2.2 *ON Impedance*

The voltage drop across the switch in the closed condition (common-emitter connection) is given by[7]

$$V_{CE} = (\pm)\frac{kT}{q}\ln\frac{\alpha_I\left(1 - \frac{I_{C1}}{I_{B1}}\left(\frac{1-\alpha_N}{\alpha_N}\right)\right)}{1 + \frac{I_{C1}}{I_{B1}}(1-\alpha_I)} \tag{3}$$

where $kT/q = 0.026$ volts at room temperature and the $(+)$ sign applies to pnp transistors and the $(-)$ sign to npn transistors.* (For current definitions see Fig. 1.) The extremely low voltages which result when the device is driven into the current saturation region are attributed to the fact that the collector junction attains a forward bias almost equal to that of the emitter junction. In order to obtain a low value of V_{CE} it is necessary to have both α_N and α_I large, approaching unity, and to maintain these values at high currents. Experience has shown that the best way to accomplish this is to use a symmetrical structure with a thin base layer.

An expression for the ac impedance of a common-emitter switch has also been derived.[7] The expression shows that if this is the switch parameter of primary importance in a given application, it may be necessary to drive the switch well into the current saturation region in addition to using a device with high α_N and α_I.

2.3. *Current Carrying Ability*

The power dissipation in a transistor switch is easily calculable provided the collector current and voltage waveforms are known. In many cases most of the power will be dissipated during the transition from

* This expression is not applicable to grown-junction transistors which may have 10 to 200 ohms of collector body resistance.

OFF to ON or vice versa. Frequently, however, the switch is maintained in the closed condition for extended periods of time. During these intervals the power dissipation is given approximately by

$$P_{dis} = I_C V_{CE} + I_B^2 r_{B3} \tag{4}$$

where V_{CE} has a value given by (3) and r_{B3} is the base resistance in the current saturation region. For large collector currents, r_{B3} may be only a fraction of the base resistance in the active region. It is apparent that the transistor should be driven well into the saturation region to obtain a low value of V_{CE}. The current carrying ability is determined primarily by the allowable power dissipation.

2.4 *Maximum Open Circuit Voltage*

The maximum open circuit switch voltage exerts a controlling influence on the choice of geometry and material constants. If sufficient collector to base voltage is applied to extend the space charge layer of the collector junction through the entire thickness of the base layer to the emitter junction "punch-through"[2] results and the emitter and collector junctions behave as if shorted together through a battery. In alloyed devices the punch through voltage is determined by the resistivity of the base material and the shortest base distance between emitter and collector.

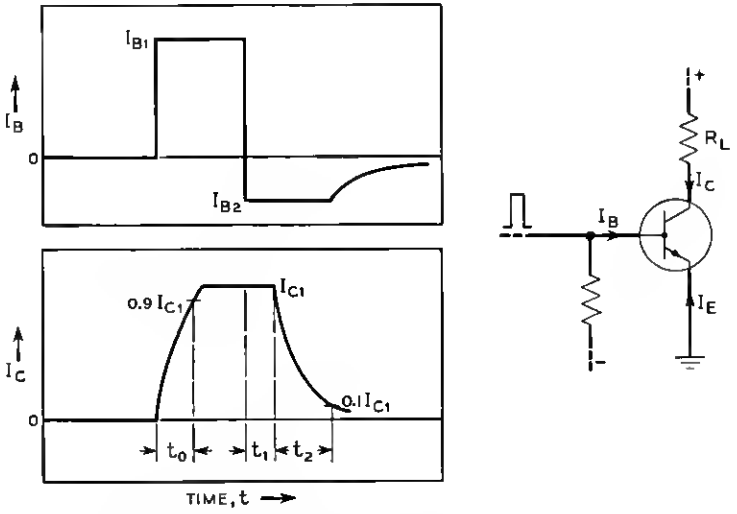

Fig. 1 — Transient behavior of common-emitter pulse amplifier.

Avalanche multiplication[3, 4] of the emitter current, which is also a function of the collector voltage, places an upper limit on the low voltage value of alpha, since at some collector voltage the value of alpha must necessarily become equal to unity[5, 6] (whether due to body or surface avalanche breakdown). This may result in improper operation* in the case of common-emitter circuits and other circuits not designed for $\alpha > 1$. The voltage at which alpha becomes one is also the maximum voltage which can be sustained from collector to emitter with the base open circuited. Avalanche multiplication is related to the body breakdown voltage which in turn is directly related to the base layer resistivity in the case of alloyed-junction transistors.

2.5 *Switching Speed*

Rise time in transistor switching circuits has been analyzed by J. L. Moll.[8] This analysis has been found to give sufficiently accurate results provided the time constant associated with the collector capacitance and load resistance is small compared with the time constant associated with the frequency cut-off of alpha, i.e., $R_L C_C < 1/\omega_N$. Rise time in the common-emitter circuit is then given by

$$t_0 = \frac{1}{(1 - \alpha_N)\omega_N} \ln \frac{1}{1 - 0.9 \dfrac{1 - \alpha_N}{\alpha_N} \dfrac{I_{C1}}{I_{B1}}} \tag{5}$$

where t_0 is the time required for the collector current to rise to 0.9 of its final value and ω_N is the angular cut-off frequency of the normal alpha. The quantity $t_0\omega_N$ is plotted in Fig. 2 as a function of α_N for various values of I_B/I_C. For sufficiently high values of alpha and sufficiently high values of I_B/I_C, the rise time is given by

$$t_0 = 0.9 \frac{1}{\omega_N \alpha_N} \frac{I_C}{I_B} \tag{6}$$

As an example, if an amplifier is to have a current gain of twenty and a rise time of a tenth of a microsecond, $f_N = \omega_N/2\pi$ must be about 30 mc./sec.

If a common-emitter pulse amplifier is driven by essentially a current source, the base resistance in the active region does not limit the response time.

* It is possible to operate transistors with alpha greater than unity in common-emitter pulse amplifier circuits. However under some driving conditions the circuit may be bistable and difficulty will be encountered in turn-off. In general, large currents may be needed for turn-off and the pulse source should have low impedance.

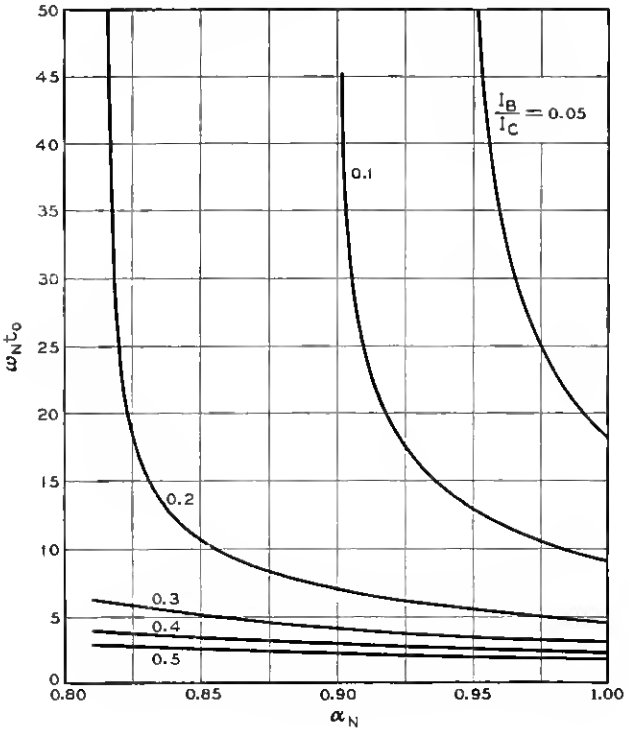

Fig. 2 — Normalized rise time as a function of alpha for common-emitter pulse amplifier.

At the termination of the input pulse the output current remains relatively constant for a certain period of time because of minority carrier storage. During this interval (t_1 in Fig. 1) the stored minority charge in the base layer is flowing out at a rate limited by the circuit resistance. Not until the minority carrier density at the base side of the collector junction has been reduced to zero by this outflow does the decay of circuit current commence (interval t_2 in Fig. 1). The storage time has been shown by Moll to be[8]

$$t_1 = \frac{\omega_N + \omega_I}{\omega_N \omega_I (1 - \alpha_N \alpha_I)} \ln \frac{I_{B1} - I_{B2}}{\frac{1 - \alpha_N}{\alpha_N} I_{C1} - I_{B2}} \tag{7}$$

This time is small if the values of normal and inverted alpha frequency cut-off are both large. The expeditious way of accomplishing this in an

alloyed structure is to make the structure symmetrical, in which case the expression for storage time becomes

$$t_1 = \frac{2}{\omega_N (1 - \alpha_N^2)} \ln \frac{I_{B1} - I_{B2}}{\frac{1 - \alpha_N}{\alpha_N} I_{C1} - I_{B2}} \tag{8}$$

Storage time is plotted in Fig. 3 as a function of alpha for a given set of current conditions for a symmetrical transistor.

Decay time is the interval of time between the end of the storage interval and the point when the load current reaches 10 per cent of its value before turn-off. It is given by

$$t_2 = \frac{1}{(1 - \alpha_N)\omega_N} \ln \frac{I_{C1} - \frac{\alpha_N}{1 - \alpha_N} I_{B2}}{0.1 I_{C1} - \frac{\alpha_N}{1 - \alpha_N} I_{B2}} \tag{9}$$

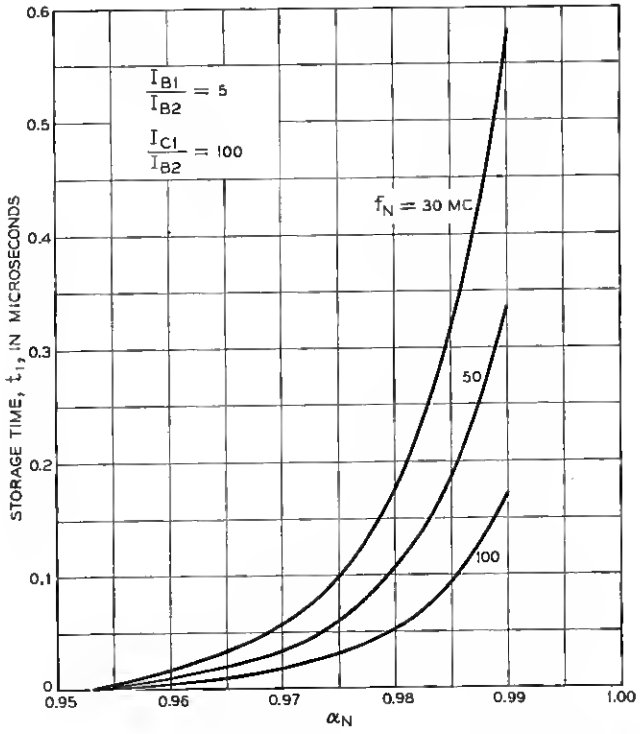

Fig. 3 — Storage time as a function of alpha for common-emitter pulse amplifier.

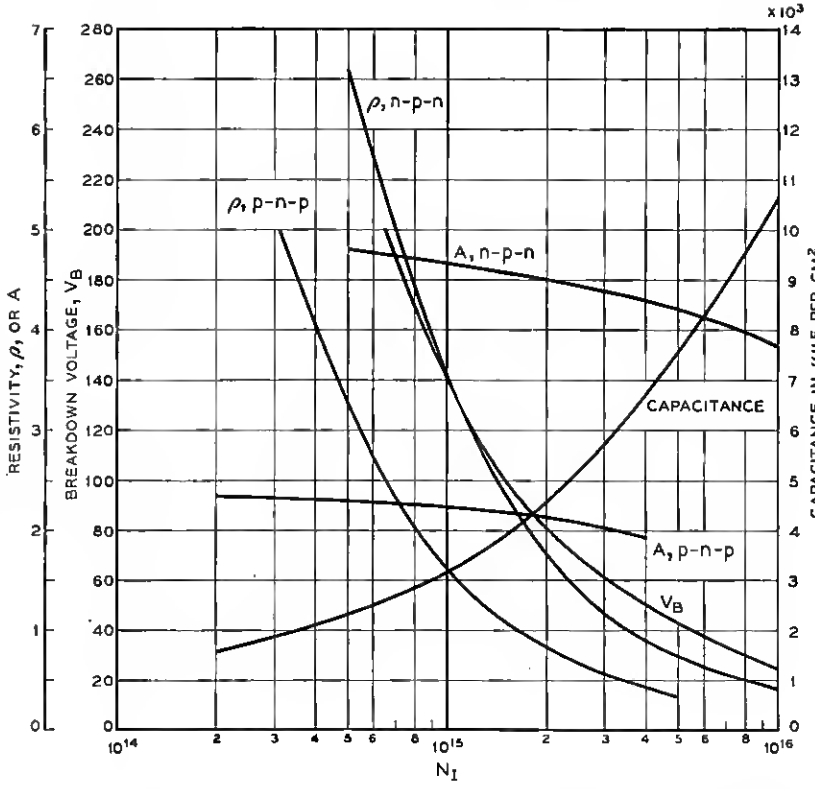

Fig. 4 — Resistivity, capacitance (at 10 *V.*) per unit area, breakdown voltage, and frequency cut-off factors versus density of impurity centers for germanium.

The time constant associated with the decay time is seen to he the same as that associated with the turn-on time. The decay time is usually somewhat larger than the rise time unless relatively large values of hase current are used during turn-off.

3.0 DEVICE DESIGN

3.1 *Junction Capacitance*

Alloyed junctions are usually ahrupt or step junctions, even though the actual junction may he formed hy the diffusion of donors or acceptors ahead of the surface of deepest penetration of the alloying material. For

step junctions of this type the junction capacitance is given by[9]

$$C = \left(\frac{\kappa\varepsilon_0 q}{2}\right)^{1/2}\left(\frac{N_I}{V}\right)^{1/2} \tag{10}$$

or, for germanium,

$$C = 3.4 \times 10^{-4}\left(\frac{N_I}{V}\right)^{1/2} \qquad \mu\mu f/cm^2 \tag{11}$$

where V is the total reverse junction bias in volts and $N_I = |N_D - N_A|$ is the net density of donors or acceptors in the base region. Capacitance per unit area is plotted in Fig. 4 as a function of N_I assuming $V = 10$ volts.

3.2 *Space Charge Layer Width*

Since the emitter and collector regions of alloyed transistors are heavily doped with donor or acceptor atoms, their conductivities are high and the space charge layer associated with the junction capacitance extends primarily into the base layer. The thickness of this space charge layer is given by[9]

$$W_S = \left(\frac{2\kappa\varepsilon_0}{q}\right)^{1/2}\left(\frac{V}{N_I}\right)^{1/2} \tag{12}$$

or, for germanium,

$$W_S = 4.2 \times 10^{3}\left(\frac{V}{N_I}\right)^{1/2} \qquad \text{cm} \tag{13}$$

The widening of the space charge layer with voltage limits the resistivity and width of the base region assuming the operating collector voltage is specified. If the base layer is sufficiently thin and of high resistivity, the space charge layer may extend over to the emitter at collector voltages below the collector breakdown voltage. The voltage at which this occurs, the punch-through voltage, is the same whether it be applied collector to base, collector to emitter, or emitter to collector. In Fig. 5 the solid curves are contours of constant space charge layer width plotted with junction voltage and base layer resistivity as the independent variables for n-p-n transistors. Similar solid curves in Fig. 6 are for p-n-p transistors. For a given maximum operating collector to base or collector to emitter voltage and a given resistivity of the base layer material these curves indicate the minimum base layer thickness that may be used if punch through is not to occur at a voltage below the given value.

3.3 *Breakdown Voltage*

The breakdown voltage of germanium step junctions when the breakdown voltage is due to avalanche multiplication within the body of the semiconductor has been investigated by S. L. Miller[5] using both alloyed junctions and junctions grown to simulate alloyed junctions. The body

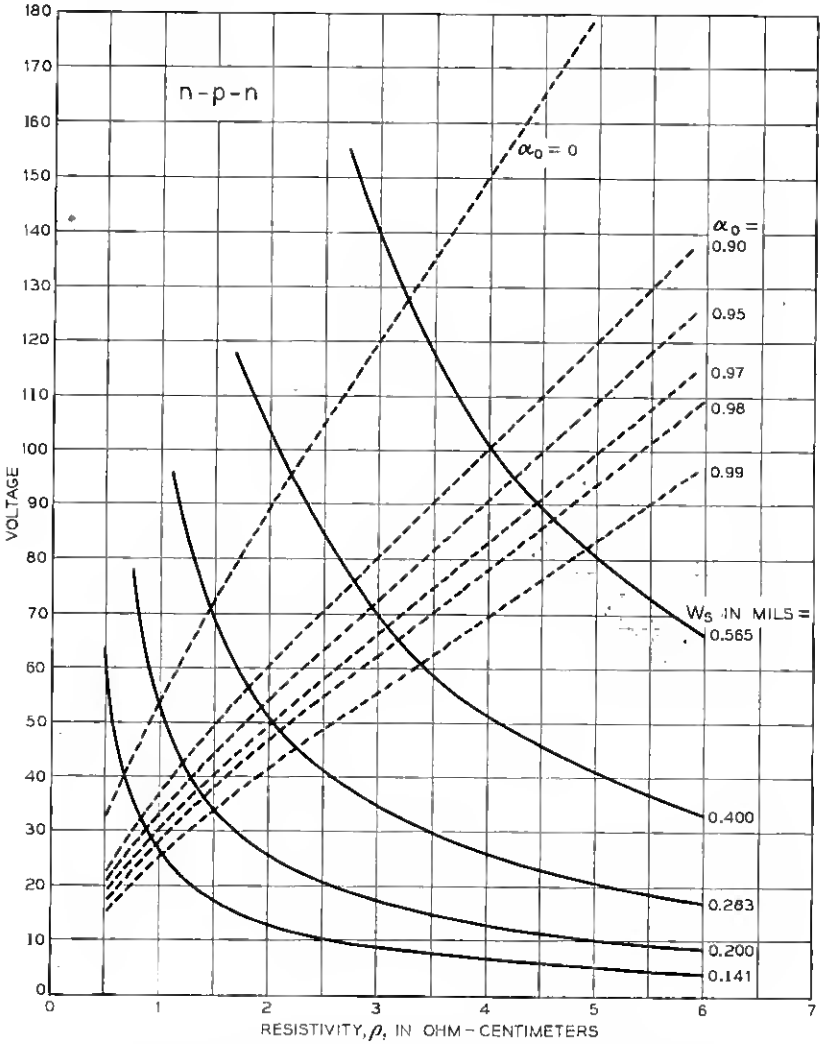

Fig. 5 — Contours of unity total alpha and constant space-charge width for n-p-n alloyed-junction, germanium transistors.

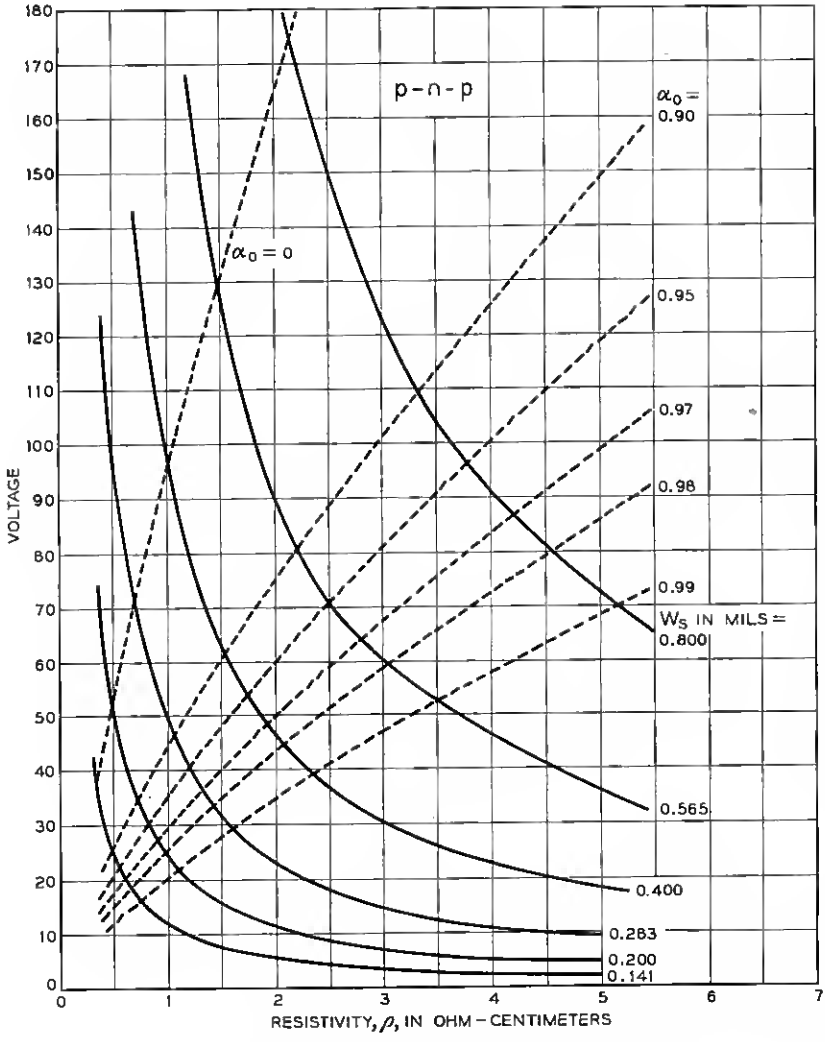

Fig. 6 — Contours of unity total alpha and constant space-charge width for p-n-p, alloyed-junction, germanium transistors.

breakdown voltage thus obtained is plotted in Fig. 4 as a function of N_I. Also plotted in this figure are curves of resistivity versus N_I^{10} for both n-type (labeled p-n-p) and p-type (labeled n-p-n) material. Body breakdown voltage for a given resistivity of base material can thus be read from these curves.

3.4 *Avalanche Multiplication*

The variation of avalanche multiplication with junction voltage for step junctions on germanium is given by the empirical equation[5]

$$M = \frac{1}{1 - (V/V_B)^n} \tag{14}$$

Since current injected by the emitter junction is multiplied by this factor upon being collected, the variation of alpha with collector voltage is given by the equation

$$\alpha = \alpha_0 M = \frac{\alpha_0}{1 - (V/V_B)^n} \tag{15}$$

when space-charge-layer widening effects[11] are neglected.

For alloyed transistors made on base material in the one to five ohm-centimeter range, values of $n = 3$ for p-n-p transistors and $n = 6$ for n-p-n transistors give multiplications which agree well with experiment.[5] Since values of alpha greater than unity may result in failure of junction transistor circuits to operate properly, it is necessary to limit the value of alpha at zero collector voltage to such a value that alpha will not become greater than unity at the maximum operating collector voltage. Alpha is known to vary with temperature and emitter current, hence it is necessary to study α_0 over the expected range of these variables. In Figs. 7 and 8 are shown typical variations of $(1 - \alpha_0)$ with current and temperature for p-n-p and n-p-n transistors of approximately the same geometry. Fortunately, most transistors of a given type made by the same processes show the same type of variation. Therefore, it should be necessary to measure α_0 only at a particular current and temperature to determine its maximum value.

It is apparent that the alpha of n-p-n transistors shows less variation with emitter current than the alpha of p-n-p transistors. Furthermore it has been found that the variation is decreased in both types as the base width is decreased.

The dotted curves in Figs. 5 and 6 are contours of constant α_0 plotted with collector voltage and base resistivity as independent variables, using (15) and appropriate values of n. For a given maximum collector operating voltage and base layer resistivity these curves show the maximum values of α_0 which can be permitted if total alpha is not to exceed unity at the chosen conditions.

The curves shown in Figs. 5 and 6 can be used in several different ways to design transistors or to determine whether or not a given set of requirements are compatible.

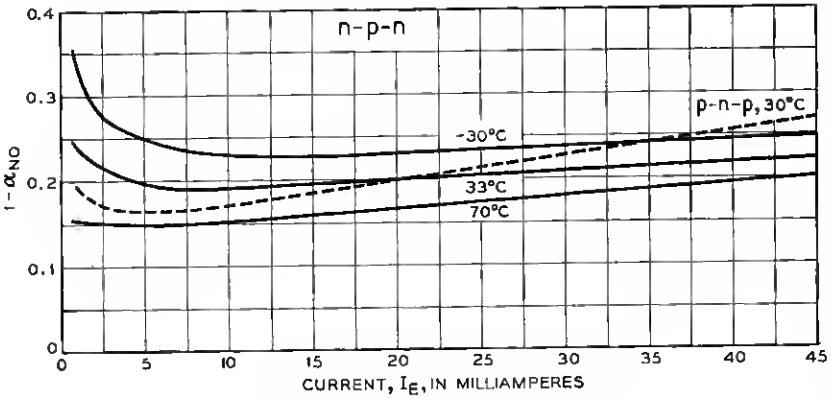

Fig. 7 — Variation of alpha with emitter current and temperature for n-p-n transistors.

3.5 *Base Resistance*

The base resistance for the somewhat idealized transistor structure shown in Fig. 9 has been calculated by J. M. Early.[11] It is given by

$$r_B = \frac{1}{8\pi}\frac{\rho}{W_1} + \frac{1}{2\pi}\frac{\rho}{W_2}\ln\left(\frac{r_2}{r_1}\right) \tag{16}$$

where the first term represents the contribution due to the base layer between the emitter and collector junctions and the second term is the contribution of the base wafer between the edge of the emitter and col-

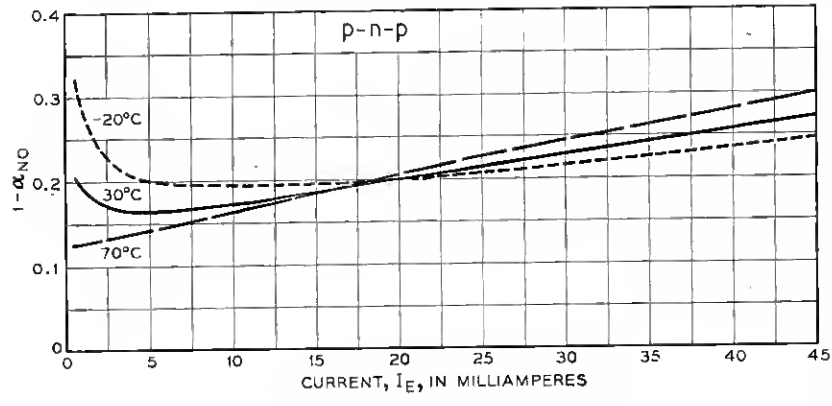

Fig. 8 — Variation of alpha with emitter current and temperature for p-n-p transistors.

lector contacts and the ring base contact. This expression is probably a good approximation to the base resistance of the transistor in the active region, particularly at low currents. As the current increases, the outer edge of the emitter becomes more forward biased than the center, thus effectively decreasing the base resistance. In the current saturation region the base resistance is given approximately by the second term, or

$$r_{B3} = \frac{1}{2\pi} \frac{\rho}{W_2} \ell n \left(\frac{r_2}{r_1} \right) \tag{17}$$

If a common-emitter amplifier is not driven from a high impedance current source, the active region base resistance may seriously limit the pulse rise time.

3.6 *Frequency Cut-Off of Alpha*

Emitted carriers cross the base layer by a diffusion process when current densities are small. Since a dispersion in transit time is inherent in such a process, changes in both magnitude and phase of alpha with frequency are to be expected.[12] The frequency at which the magnitude of alpha falls to $1/\sqrt{2}$ of its low frequency value is given by

$$f_N = \frac{D}{\pi W^2} \tag{18}$$

where D is the diffusion constant for injected carriers. This can be expressed as

$$f_N = \frac{A}{W^2} \qquad \text{mc/sec, where } W \text{ is in mils} \tag{19}$$

The variation of A with the resistivity of the base layer for alloyed-junc-

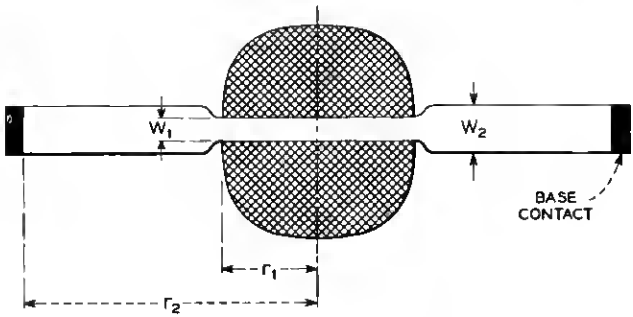

Fig. 9 — Alloyed transistor geometry.

tion germanium transistors is shown in Fig. 4 for both n-p-n and p-n-p transistors. The variation is due to mobility changes.[10]

It is of course true that at high current densities there is a departure from pure diffusion of minority carriers because of induced drift fields.[13, 14] Furthermore, at high currents the effective base layer width changes as a result of a re-distribution of emitter current. There is also a large body of evidence for anomalous changes of frequency cut-off of alpha with surface changes. However, it will be assumed that (18) is a valid criterion for frequency cut-off at low voltages and currents.

Because of space charge layer widening, the cut-off frequency of alpha should vary with collector voltage. Using (13) and (19) this variation can be shown to be given by

$$f_N = \frac{f_{N_0}}{\left[1 - \left(\frac{V_C f_{N_0}}{3.65 \times 10^{-13} N_I A}\right)^{1/2}\right]^2} \tag{20}$$

where f_{N_0} is the cut-off frequency at zero voltage. For n-p-n transistors made on 1.5 ohm-cm material

$$f_N = \frac{f_{N_0}}{[1 - 0.016(V_C f_{N_0})^{1/2}]^2} \tag{21}$$

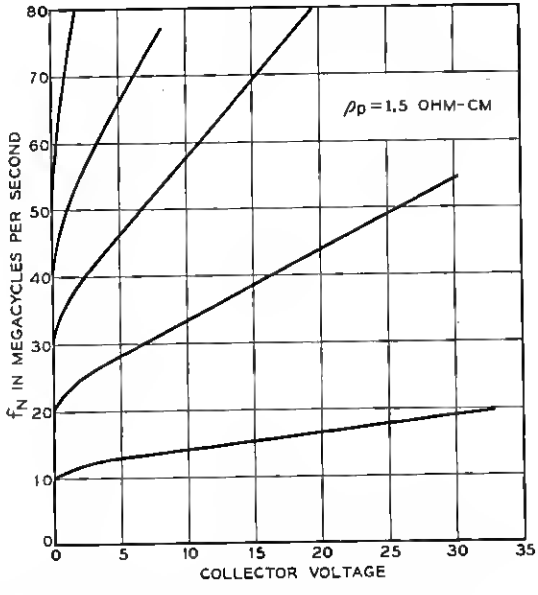

Fig. 10 — Variation of frequency cut-off of alpha with collector voltage for n-p-n transistors made on 1.5 Ω-cm Ge.

The variation of alpha cut-off frequency for alloyed junction n-p-n transistors made on 1.5 ohm-cm germanium is plotted in Fig. 10 for several values of f_{N_0}. Fig. 11 is a more general plot for other resistivities and f_{N_0}'s. It is apparent that a problem exists in alpha cut-off frequency measurement as a result of the large variation of f_N with voltage. Furthermore an exact analysis of rise time and decay time would have to take this variation into account.

It is possible that this increase of f_N with voltage may allow some relaxation of low-voltage requirements in this respect.

3.7 DISCUSSION

Let it be assumed that a transistor is desired which will operate at a collector voltage of 30 volts and which, when used as a common-emitter pulse amplifier will give a current gain of twenty with a pulse rise time of a tenth of a microsecond or less. The maximum current will be assumed to be 100 milliamperes, corresponding to a load impedance of 300 ohms.

A reasonable range for α_0 would be from 0.97 to 0.99, the maximum limit being imposed because of avalanche multiplication. From Fig. 2 it

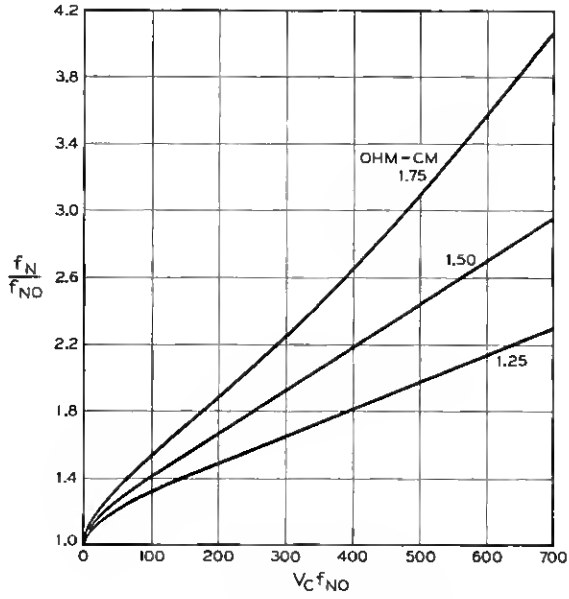

Fig. 11 — Variation of frequency cut-off of alpha with collector voltage for n-p-n transistors.

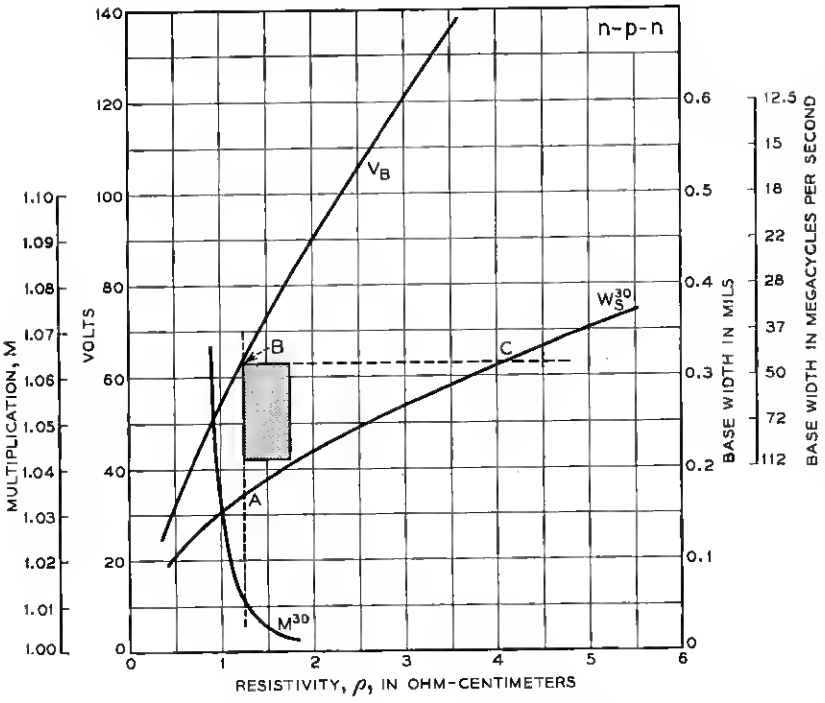

Fig. 12 — Design summary for n-p-n transistors.

is calculated that the minimum allowable value of f_N is 43 mc/sec. From Fig. 5 (for n-p-n transistors) assuming a maximum collector voltage of 30 volts and a maximum permissible α_0 of 0.99 it is seen that the resistivity of the base material must he at least 1.25 ohm-cm and that the minimum hase layer thickness is about 0.175 mils, corresponding to a f_N of 144 mc/sec from (19) and Fig. 4. Unfortunately, it is difficult with the design data plotted as they are in Fig. 5 to obtain the limits on the hase resistivity and the lower limit on base width which are necessary to insure freedom from punch through and alpha greater than unity for a specified collector voltage. For this reason the design data have been replotted in a different manner in Figs. 12 and 13. Here the avalanche multiplication factor M and space charge layer width W_s, both at 30 volts, have been plotted as a function of base layer resistivity. Again assuming a maximum α_0 of 0.99 this places an upper limit of 1.01 on the multiplication and therefore, a lower limit of 1.25 ohm-cm on the base layer resistivity. Since the base layer width must be greater than the

space charge layer width the range of base layer width chosen must lie entirely above the curve for space charge layer width at 30 volts. In addition, the minimum frequency cut-off requirement of 43 mc/sec means the design must lie below the horizontal dotted line. Thus triangle ABC encloses the region of possible designs. The shaded rectangle seems to be the most appropriate design. The frequency range can be read directly from the base width scale since this scale has been calibrated in mc/sec. Assuming a 0.015″ diameter collector junction, this design can be summarized as follows:

Base layer resistivity — 1.25 to 1.75 ohm-cm
Base layer width — 0.21 to 0.32 mils
Collector capacitance (10V) — 5.5 to 6.4 $\mu\mu$f
Alpha — 0.97 to 0.99
Frequency cut-off of alpha — 43 to 100 mc/sec

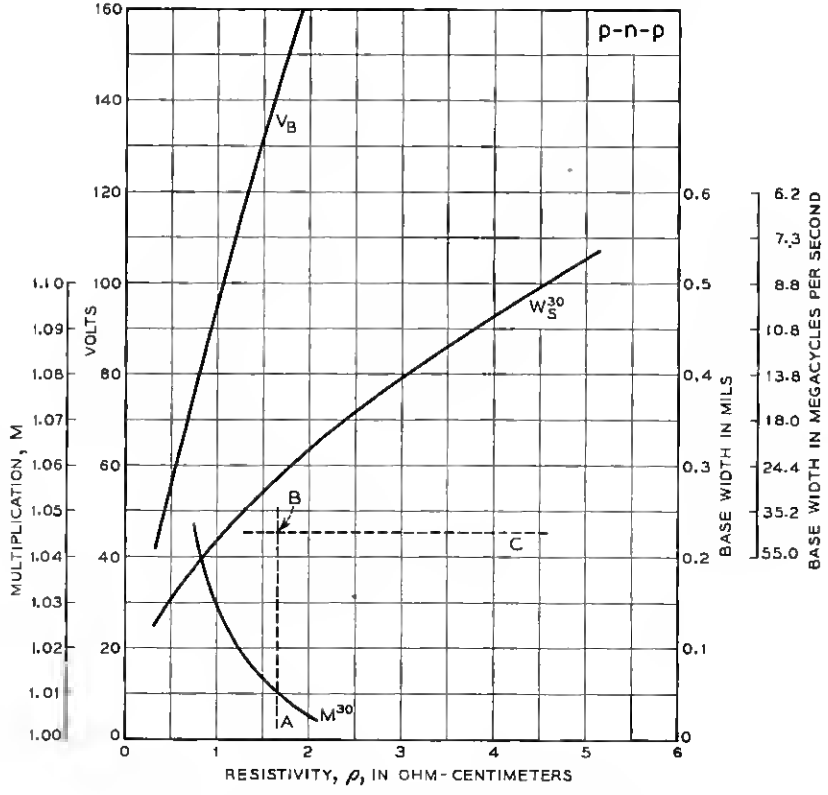

Fig. 13 — Design summary for p-n-p transistors.

By studying the data in Figs. 6 and 13 for p-n-p transistors it is seen that a design to meet the stated requirements is not possible. Assuming a maximum collector voltage of thirty volts, the absolute maximum value of cut-off frequency would he about 27 mc/sec for p-n-p transistors.

Returning to the n-p-n design, assume that the device has the following geometry:

Emitter dia — 0.015″
Collector dia — 0.015″
Base layer width — 0.00025″
Base wafer width — 0.0015″
Base contact dia — 0.030″
Base resistivity — 1.5 ohm-cm

then from (16) and (17), $r_B = 138$ ohms and $r_{B3} = 44$ ohms. The collector capacitance at 10 volts is 5.8 $\mu\mu$f. For a load resistance of 300 ohms, $R_L C_C = 1.7 \times 10^{-9}$ sec which is not very small compared to $1/\omega_N = 3.7 \times 10^{-9}$ sec. If the base is driven hy a current source whose internal impedance is large compared with 138 ohms, the rise time would probably be controlled by the alpha cut-off frequency, however.

4.0 CONCLUSIONS

(1) The interdependence of transistor parameters has heen shown to set theoretical limits on designs which are possible. In essence, high frequency and high voltage requirements militate against each other. A design theory which takes these factors into account has been described.

(2) For high-speed and high-voltage switching (and transmission) applications, it is shown that the n-p-n enjoys a superiority beyond that expected from only mobility considerations. The additional advantage stems from the different multiplication laws for n-p-n and p-n-p transistors. For example, it is theoretically feasible to make alloyed junction n-p-n transistors with alpha cut-off frequencies in the range of 50 to 100 mc/sec which will sustain collector voltages as high as 30 volts, and be capable of operating as pulse amplifiers in circuits with a current gain of 20 and a pulse rise time of less than a tenth of a microsecond. A design meeting these requirements is not possible with p-n-p's. In the example chosen, there is a ratio of 5.3 between the maximum frequency cut-off of alpha obtainable with n-p-n transistors as compared with p-n-p transistors for the same maximum value of low voltage alpha.

The design theory developed above gives upper limits on what can be achieved. It has been assumed that there are no fabrication problems and that geometries are ideal, namely, that the junctions are perfectly

planar and parallel. Furthermore, it has been assumed that the breakdown and multiplication properties of collector junctions are determined by the bulk properties of the junction. In many cases there are breakdowns on the surface at lower voltages. These are frequently multiplicative but they multiply a very small fraction of the emitter current.

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REFERENCES

1. Early, J. M., p-n-i-p and n-p-i-n Junction Transistor Triodes, B.S.T.J., **33**, pp. 517–533, May, 1954.
2. Shockley, W., Transistor Electronics — Imperfections, Unipolar and Analog Transistors, Proc. I.R.E., **40**, pp. 1289–1313, Nov., 1952.
3. McKay, K. G., and McAfee, K. B., Electron Multiplication in Silicon and Germanium, Phys. Rev., **91**, pp. 1079–1084, Sept. 1, 1953.
4. McKay, K. G., Avalanche Breakdown in Silicon, Phys Rev, **94**, pp. 877–884, May, 15, 1954.
5. Miller, S. L., Avalanche Breakdown in Germanium, Phys Rev, to be published.
6. Miller, S. L., and Ebers, J. J., Alloyed Junction Avalanche Transistors, B.S.T.J., to be published.
7. Ebers, J. J., and Moll, J. L., Large-Signal Behavior of Junction Transistors, Proc. I.R.E., **42**, pp. 1761–1772, Dec., 1954.
8. Moll, J. L., Large-Signal Transient Response of Junction Transistors, Proc. I.R.E., **42**, pp. 1773–1784, Dec., 1954.
9. Shockley, W., The Theory of p-n Junctions in Semiconductors and p-n Junction Transistors, B.S.T.J., **28**, pp. 435–489; July, 1949.
10. Prince, M. B., Drift Mobilities in Semiconductors, I. Germanium, Phys Rev, **92**, pp. 681–687, Nov., 1, 1953.
11. Early, J. M., Design Theory of Junction Transistors, B.S.T.J., **32**, pp. 1271–1312, Nov., 1953.
12. Shockley, W., Sparks, M., and Teal, G. K., p-n Junction Transistors, Phys Rev, **83**, pp. 151–162, July 1, 1951.
13. Rittner, E. S., Extension of the Theory of the Junction Transistor, Phys Rev, **94**, pp. 1161–1171, June 1, 1954.
14. Webster, W. M., On the Variation of Junction Transistor Current Amplification Factor with Emitter Current, Proc. I.R.E., **42**, pp. 914–920, June, 1954.